REMARKS

Claims 1-3, 6-13, 15-27 and 32-39 are present in this case. Claims 4, 5, 14, 28-31 and 40 have been indicated canceled by the above-proffered amendment and claims 1, 23, 26, 27 and 38 have been amended.

The Examiner rejected claims 1, 23, 26, 27 and 38 under 35 U.S.C. 112 second paragraph as being incomplete for omitting essential structural cooperative relationship of elements. This ground of rejection has been avoided by amendment of these claims. The same is true with respect to the rejection of the dependent claims.

The Examiner has rejected claims 1, 23, 26, 27 and 38 as well as the claims dependent thereon in that the term "time integrators" in "a plurality of time integrators gated to generate a plurality of time-integrated signals in response to said at least one pulse-position modulated signal and said plurality of coordinating clock signals (lines 6-9)" makes is vague and unclear. It is not clear which term "time integrators" is referring to." The objection that it is not clear what term "time integrators" is referring to is not deemed merited. As the specification and drawings make clear, for example, paragraph 0027 describes the time-interleaving integrator circuit 76 which "includes multiple phase integrators 78. Each integrator 78 includes an integrator input 80, a hold input 82, a reset terminal 84, and an output 86. The integrator inputs 80 and the reset terminals 84 are coupled to the clock circuit outputs 72. Each of the hold inputs 82 are coupled to the second timer circuit output 66. The outputs 86 are coupled to the switches 88. The integrators 78 have analog output signals IntA, IntB, and IntC, respectively. Each integrator 78 may operate in an integration mode, a hold mode, or a reset mode..." The specification at paragraph 0030 details further the arrangement involved. It is clear when

the claim is read against the disclosure that the skilled in the art would have no difficulty with the term "time integrators" and what it is referring to.

As amended, the invention "provides a communication system and method of extracting information from pulse-position modulated (PPM) signals. A communication receiver is provided and includes a data receiver that receives a pulse-position modulated signal. A clock circuit separates a reference clock signal into multiple coordinating clock signals. Multiple time integrators are gated to generate multiple time-integrated signals in response to the pulse-position modulated signal and the coordinating clock signals. A combiner forms a demodulated signal from the time-integrated signals." (paragraph 0008).

The communication system of the invention has numerous advantages, as for example, set forth in paragraphs 0009-0012 of the application.

The rejection of claims 1, 23, 26, 27 and 38 under 35 U.S.C. 102(b) as being anticipated by Ohtani (5691665) is not well taken.

The Ohtani device, namely a PPM demodulation device, differs in its objectives and its structure for achieving such objectives. The Ohtani PPM demodulation device is intended for use in optical communications for demodulating reception data that is subjected to pulse-position modulation with a pulse signal inserted into a predetermined symbol position.

According to Ohtani, a PPM signal 21 of a digital signal level is applied to a clock reproduction unit 11 and a sample result holding unit 12. A master clock signal 42 is applied to clock reproduction unit 11 from an external crystal oscillator 33. Clock reproduction unit 11 provides a reproduced clock signal 22 from received PPM signal 21

according to master clock signal 42. Reproduced clock signal 22 is applied to sample result holding unit 12, a symbol synchronizing signal generation unit 14, a reception data reproduction unit 15, and a reception data processing unit 34 (refer to column 5, lines 3-13).

In Ohtani, sample result holding unit 12 samples PPM signal 21 according to reproduced clock signal 22 to hold a sample result 23. Sample result 23 is applied to symbol synchronizing signal generation unit 14 and reception data reproduction unit 15. Symbol synchronizing signal generation unit 14 achieves symbol synchronization from sample result 23 according to reproduced clock signal 22. The obtained symbol synchronizing signal 25 is applied to reception data reproduction unit 15 and reception data processing unit 34. Reception data reproduction unit 15 demodulates reception data according to sample result 23, symbol synchronizing signal 25, and reproduced clock signal 22. More specifically, reception data reproduction unit 15 analyzes the result of a plurality of previous samples from sample result 23 to demodulate reception data according to a specific procedure. Symbol synchronizing signal 25, demodulated data 26, and reproduced clock signal 22 are applied to reception data processing unit 34 to be processed (refer to column 5, lines 14-31).

In Ohtani, the sample result holding unit 12 is formed of D type flipflops 121, 122, 123, . . . 12n connected in series. PPM signal 21 is applied to the D input of the first D type flipflop 121. Reproduced clock signal 22 is applied to the clock input terminal of each of D type flipflops 121, 122, 123, . . . , 12n. Sample result 23 is provided from each of D type flipflops 121, 122, 123, . . . 12n. This sample result 23 is used for symbol synchronizing signal generation unit 14 to recognize a start flag pattern, and for reception

data reproduction unit 15 to determine reception data. Symbol synchronizing signal generation unit 14 requires a sample result 23 corresponding to the length of the start flag pattern. For example, when the start flag pattern shown in the timing chart of FIG. 19 (pattern of the shaded portion of transmission PPM waveform) is to be used, the pattern is represented as "1000 0000 1001 1000" in pulse slot unit. Therefore, sixteen sample results 23 must be applied from sample result holding unit 12 to symbol synchronizing signal generation unit 14. Reception data reproduction unit 15 can carry out demodulation referring to sample results (refer to column 5, line 50 to column 6, line 4).

The Examiner in analyzing Ohtani regarding claim 1 identifies the "plurality of coordinating clock signals (clock inputs of 121, 122… in Fig.3); a plurality of time integrators gated (Fig. 3: 121, 122…)." As can be appreciated from the Ohtani disclosure, reference numerals 121, 122 and 123 are each D type flipflops and there applied thereto either the PPM signal 21 or the clock signal 22 to provide the sample result. The sample result holding unit is critical to the Ohtani invention.

There is no provision or requirement for such a unit or its function in the invention. The Ohtani reference does not teach or suggest applicant's invention.

The same is true for claims 23, 26, 27 and 38 all of which are independent claims and which as in claim 1 do not require the sample result holding unit or for that matter sample results.

This feature is also not found in any of the dependent claims so that they in addition to the independent claims should be allowed to applicants.

Respectfully Submitted,
Attorney for Applicant

Dated: November 2, 2007

/evelyn m. sommer/

Evelyn M. Sommer
Registration No. 19,603
Joshua S. Broitman
Registration No. 38,006
OSTRAGER CHONG FLAHERTY AND BROITMAN, PC
570 Lexington Avenue, 17th Floor
New York, NY 10022-6894
Phone: (212) 681-0600
Customer Number: 64722